ACS APPLIED MATERIALS & INTERFACES

Research Article

www.acsami.org

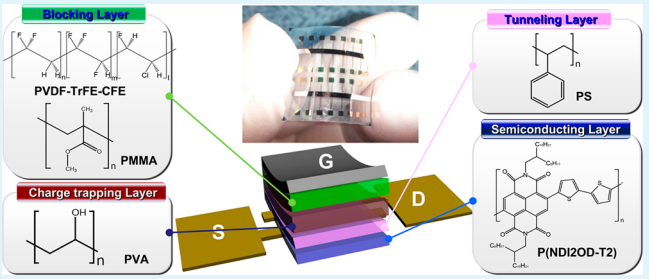
Highly Reliable Top-Gated Thin-Film Transistor Memory with Semiconducting, Tunneling, Charge-Trapping, and Blocking Layers All of Flexible Polymers

Wei Wang, Sun Kak Hwang, Kang Lib Kim, Ju Han Lee, Suk Man Cho, and Cheolmin Park*

Department of Materials Science and Engineering, Yonsei University, 50 Yonsei-ro, Seodaemun-gu, Seoul, 120-749, Republic of Korea

Supporting Information

ABSTRACT: The core components of a floating-gate organic thin-film transistor nonvolatile memory (OTFT-NVM) include the semiconducting channel layer, tunneling layer, floating-gate layer, and blocking layer, besides three terminal electrodes. In this study, we demonstrated OTFT-NVMs with all four constituent layers made of polymers based on consecutive spin-coating. Ambipolar charges injected and trapped in a polymer electret charge-controlling layer upon gate program and erase field successfully allowed for reliable bistable channel current levels at zero gate voltage. We have observed that the memory performance, in particular the reliability of a device, significantly depends upon the thickness of both blocking and tunneling layers, and with an optimized layer thickness and materials selection, our device exhibits a memory window of 15.4 V, on/off current ratio of 2×10^4, read and write endurance cycles over 100, and time-dependent data retention of 10^8 s, even when fabricated on a mechanically flexible plastic substrate.



KEYWORDS: *nonvolatile memory, thin-film transistor memory, polymer memory, polymer charge-trapping layer, polymer tunneling and blocking layers, sequential spin-coating*

1. INTRODUCTION

Organic memories have attracted extensive research interest for their many advantages over their inorganic counterparts, including low cost, light weight, mechanical flexibility, and low-temperature processing.[1−14] Among the many device configurations of organic memories, a nonvolatile memory (NVM) based on an organic thin-film transistor (OTFT) architecture with a floating-gate (FG) is considered as a promising candidate for next-generation organic flash memory due to its simple device structure of single-transistor, nondestructive read-out, and compatibility with complementary logic circuits. Great efforts have been made to develop efficient floating-gate layers suitable for OTFT configurations. OTFT-NVMs are representative of floating-gate layers containing thermally evaporated metal (e.g., Au, Ag, and Al) nanoparticles (NPs) in vacuum.[1−5] Using high vacuum is, however, undesirable for large-area and low-cost memories, in particular, based on printing technologies. Although various floating-gate layers consisting of solution-processed metal NPs have also been developed by an electrostatic self-assembly method,[6−8] synthesis in a block copolymer,[9,10] and microcontact printing,[11] the formation of uniform metal NPs in both size and distribution was not straightforward and often required elaborate control of process parameters.[12−14]

Alternatively, polymer electret layers have been introduced to act in a role similar to a floating-gate, with their great advantage of facile fabrication of homogeneous and uniform films by spin-coating.[14−23] There are, however, several technological issues that still limit the full realization of the memory performance of OTFT-NVMs with polymer electrets. First of all, the majority of previous works employed bottom gate architectures with thermally evaporated organic semiconducting layers to avoid a possible intermixing between semiconductor and gate insulator that might occur with solution-processed semiconductors.[2−4,6−13,15−23] Not to mention thermally evaporated semiconductors, top-gate OTFT-NVMs are more desirable for reliable operation due to the autoencapsulation of air-sensitive organic semiconductors by the overlaid gate insulator. Only a few top-gate OTFT-NVMs have been reported with floating-gate layers of thermally evaporated metal NPs.[1,5,24]

Further materials design should be made in the development of top-gate OTFT-NVMs containing solution-processed polymer charge-trapping layers. Since charge-trapping and detrapping dominantly occur at the surface of a polymer electret, a four stacked layer structure, including active layer, tunneling layer, charge-trapping layer, and blocking layer, is in high demand for reliable memory operation. In particular, trapped charges can remain stable at the interface between the tunneling and charge-trapping layer due to an efficient physical barrier of the tunneling layer from the semiconductor. In fact,

Received: March 13, 2015
Accepted: May 6, 2015
Published: May 6, 2015

DOI: 10.1021/acsami.5b02213
ACS Appl. Mater. Interfaces 2015, 7, 10957−10965

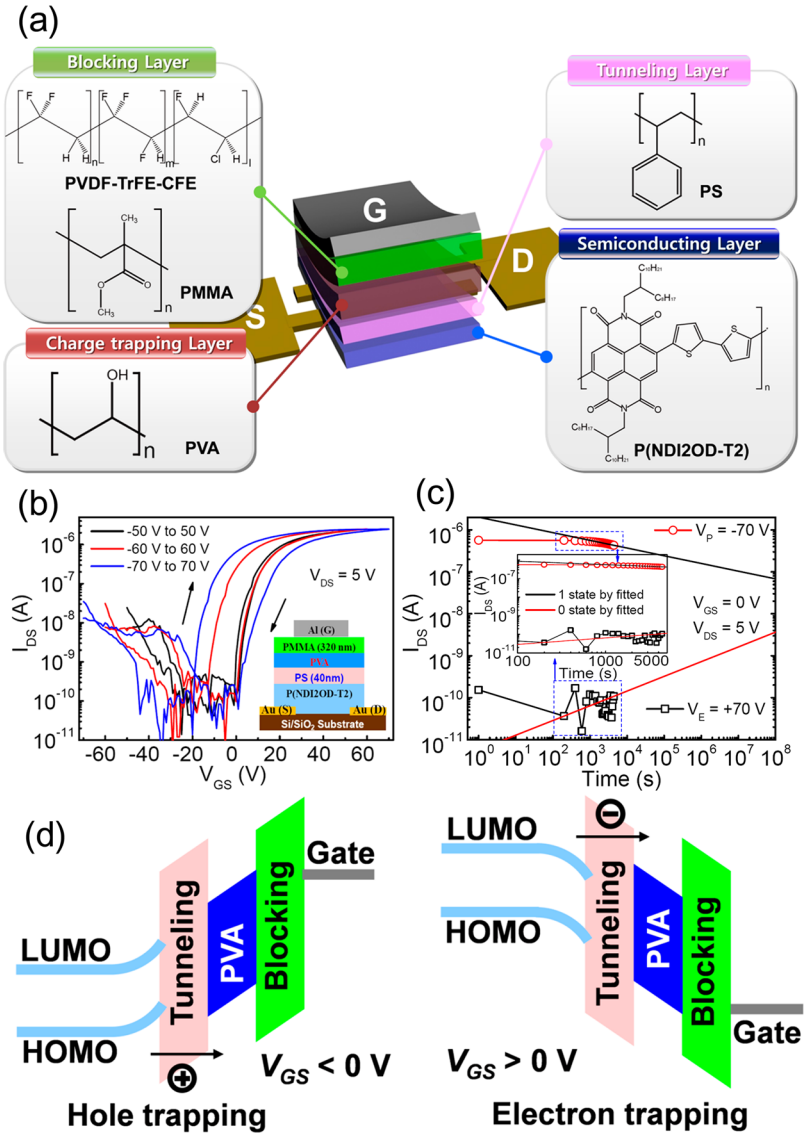


Figure 1. (a) Schematic diagram of the top-gate OTFT-NVM with all-polymer semiconducting, tunneling, charge-trapping, and blocking layers. The chemical structures of the materials used in the study are also shown. (b) Transfer characteristics at different V_{GS} sweeping ranges and (c) memory retention characteristics at both "1" and "0" states of a typical top-gate OTFT-NVM on the Si substrate. The inset of part b shows the schematic configuration of the OTFT-NVM. The inset of part c is a magnified display of the experimental data up to 5000 s and fitted data of the retention. (d) Energy band diagrams of the charge-trapping mechanisms.

previous top-gate OTFT-NVMs with solution-processed polymer charge-trapping layers were not sufficiently reliable due to the absence of the tunneling layer in the memory architecture.[14,25] Construction of all four solution-processed polymer layers suitable for high-performance top-gate OTFT-NVMs is still challenging. This requires resolving numerous materials and process issues, such as selection of solvents, control of each layer thickness and morphology, and development of firm materials interfaces.

Here, we report high-performance top-gate OTFT-NVMs with four functional polymer layers of semiconducting channel, tunneling, charge-trapping, and blocking layer stacked from bottom to top prepared by consecutive spin coating of each polymer solution. A polymer electret, poly(vinyl alcohol) (PVA), was employed and sandwiched between the dielectric tunneling and blocking polymer layers. Excellent charge-trapping and detrapping in the polymer electret optimized by types of polymers and their film thickness of both tunneling and blocking layers allowed for realization of a highly reliable and robust memory, with a high on/off memory current ratio $>10^4$, write/read cycle endurance over 100 times, and long retention ability of 10^8 s. Furthermore, a device fabricated on a mechanically flexible polymer substrate again exhibits that the memory performance comparable with that on a Si substrate was rarely altered, even after 1000 inner and outer bending events at a bending radius of 5.8 mm.

2. EXPERIMENTAL SECTION

Materials. Poly{[*N*,*N*′-bis(2-octyldodecyl)naphthalene-1,4,5,8-bis(dicarboximide) -2,6-diyl]-*alt*-5,5′-(2,2′- bithiophene)} [P(NDI2OD-T2)] (N2200) was purchased from Polyera Corp. and used without purification. PVA (M_n = 31−50 kg mol^{-1}), polystyrene (PS) (M_n = 28 kg mol^{-1}), and poly(methyl methacrylate) (PMMA) (M_n = 12 kg mol^{-1}) were purchased from Sigma-Aldrich. Poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) [P(VDF-TrFE-CFE)] (standard composition) terpolymer was purchased from Piezotech-Arkema Corp.

DOI: 10.1021/acsami.5b02213
ACS Appl. Mater. Interfaces 2015, 7, 10957−10965

Device Fabrication. It is notable that any contiguous two dielectrics were prepared from the orthogonal solvents, which is important for the preparation of the present multilayer film structure by an all-solution process. The semiconductor polymer P(NDI2OD-T2) was dissolved in toluene with a concentration of 1 wt %. PS and PMMA polymers were dissolved in butyl acetate. PVA was dissolved in deionized (DI) water with a concentration of 5 wt %. P(VDF-TrFE-CFE) was dissolved in methyl ethyl ketone. Various PS, PMMA, and P(VDF-TrFE-CFE) solutions were prepared with different concentrations to get various film thicknesses.

Au film (30 nm) was thermally evaporated on the surfaces of a 200 nm thick SiO_2 insulator coated Si substrate or a flexible PES substrate as source and drain electrodes through a shadow mask. The channel length (L) and width (W) were 100 and 1000 μm, respectively. The polymers P(NDI2OD-T2), PS (or PMMA), PVA, and PMMA (or P(VDF-TrFE-CFE)) were spin-coated in sequence at a constant speed of 2000 rpm, to form the active layer, tunneling layer, charge-trapping layer, and blocking layer, respectively. The thickness of each layer was determined by the corresponding concentration of the solution. The annealing time of the tunneling layer, charge-trapping layer, and blocking layer was 0.5, 4, and 3 h, respectively, at 110 °C to evaporate the solvents. Then, 80 nm thick Al gate electrodes were evaporated on the blocking layer through a shadow mask. Finally, all devices were patterned by oxygen plasma etching.

Device Characterization. The fabricated OTFTs and OTFT-NVMs were characterized with semiconductor parameter analyzers (E5270 Agilent Technologies and Keithely 4200) in the ambient atmosphere at room temperature. The thickness of the each polymer layer was measured using an Alpha-Step 500 surface profiler (AS500) (KLA-Tencor Co.). The field effect mobility of each transistor was calculated in the linear region (V_{DS} = 5 V) with the following equation:

$$I_{DS} = \frac{W}{L}\mu C_i\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \quad (1)$$

for the trilayer gate dielectric

$$C_i = \frac{\varepsilon_0}{d_1/\kappa_1 + d_2/\kappa_2 + d_3/\kappa_3} \quad (2)$$

3. RESULTS AND DISCUSSION

As a representative polymer electret, water-soluble poly(vinyl alcohol) (PVA) is beneficial due to its excellent organic solvent resistance, which permits us to employ various dielectric polymers as the bottom tunneling as well as the top blocking layer. P(NDI2OD-T2) (N2200), used as a channel layer, shows high solubility in common organic solvents and good stability in air with a sufficiently high electron mobility of 0.45−0.85 $cm^2\ V^{-1}\ s^{-1}$.[26] In addition, the ambipolar charge transportation characteristics of P(NDI2OD-T2) arising from its polymer backbone with alternately placed electron-donor and electron-acceptor moieties[24,27] are favorable for the active layer, since ambipolar injection allows for efficient program and erase by readily overwriting the trapped charges with opposite polarity charges.[28] The structure schematic of our OTFT-NVM is shown with PS as a tunneling layer and either P(VDF-TrFE-CFE) or PMMA as a blocking layer in Figure 1a. A detailed description of the fabrication process is given in the Experimental Section. The atomic force microscopy (AFM) images confirmed that each constituent layer was smooth and pinhole-free with its root-mean-square (rms) roughness being less than 1 nm, as shown in Figure S1 (Supporting Information, SI). The PVA surface, however, shows very small dots evenly distributed with their height being approximately 5 nm, which may be tiny crystals of PVA.[29,30]

The electrical transfer characteristics of an OTFT-NVM were measured by applying various bidirectional gate-source voltages (V_{GS}) and sweeping ranges in the linear region with a constant drain-source voltage (V_{DS}) of 5 V, as shown in Figure 1b. The electron mobility (μ_e) and the subthreshold sway (SS) for the device in n-channel mode were calculated to be approximately 0.18 $cm^2\ V^{-1}\ s^{-1}$ and 0.73 V/decade in the linear region, respectively, and these values were almost independent of the variation of both V_{GS} sweeping direction and V_{GS} sweeping ranges, which suggests that the density of electron traps was not changed at the interface of P(NDI2OD-T2)/PS during operation.

Hysteresis loops were obtained, i.e., there were large shifts in the threshold voltage (V_T) between the forward and the reverse V_{GS} sweepings (Figure 1b) arising from the charges trapped in PVA layer. In order to rule out a possible charge-trapping in the PS layer rather than the PVA one,[14,31] we examined two transistors with PVA/PMMA and PS/PMMA bilayer dielectric layers. The OTFT with a PVA/PMMA bilayer dielectric exhibited a prominent hysteresis with ΔV_T of 48.5 V at a V_{GS} sweeping range of ±60 V (Figure S2a, SI) while no hysteresis was observed in the device with a PS/PMMA bilayer dielectric (Figure S2b, SI). The negligible hysteresis of the device with PS/PMMA is due to an electric field inadequate to overcome the injection barrier.[24] In our case, the electric field calculated was approximately 2.16 MV/cm at the V_G of ±60 V, which may be insufficient for charge injection. To confirm our argument, we examined another device with a thin PS(20 nm)/PMMA(100 nm) bilayer dielectric, and the results show that some hysteresis was developed upon the dual V_G sweep of ±40 V corresponding to an electric field of approximately 4.2 MV/cm (Figure S2c, SI).

The asymmetric V-shaped transfer curves observed in Figure 1b indicate ambipolar charge (electrons and holes) transportation in the channel. The larger hysteresis in the right-hand side suggests the dominant accumulation and transportation of electrons in the device. It should be also noted that the ambipolar charge transportation allows for bipolar charge-trapping and detrapping in our device, which is more beneficial than the floating-gate OTFT memories devices based on the unipolar model. When we employed a p-type P3HT as the active layer, a typical transfer hysteresis curve shows that both the programmed and erased V_T were negative due to the unipolar operation with only hole trapped and detrapped in/from the PVA layer, giving rise to a relatively small memory window (Figure S3a, SI). The results clearly suggest the importance of the minority carriers trapped in the floating-gate (or charge-trapping layer). Figure 1d shows the schematic illustration of the energy band structure of our memory. Holes/electrons were injected and trapped in the PVA layer from the semiconductor layer through the tunneling layer at negative/positive V_{GS}, respectively. The injected holes overwrote the previous trapped electrons in the PVA layer or vice versa. The holes or electrons trapped in the PVA layer induced a built-in field with a reverse direction to the supplied gate field, resulting in clockwise hysteresis.[20,32] The superimposition of both fields gave rise to two prominent, different current levels in the channel at the same V_{GS} and V_{DS}, i.e., Boolean "1" and "0" states of the memory.

The memory window (ΔV_T) increases with the V_{GS} sweeping range, as shown in Figure 1b. The stored charge density is determined by the induced memory window and can be calculated from the equation

$$\Delta V_T = Q/C_i \quad (3)$$

DOI: 10.1021/acsami.5b02213
ACS Appl. Mater. Interfaces 2015, 7, 10957−10965

Table 1. Memory Characteristics of the Top-Gate OTFT-NVMs with All-Polymer Semiconducting, Tunneling, Charge-Trapping, and Blocking Layers[a]

substrate	device architecture	thickness (nm)	mobility ($cm^2\ V^{-1}\ s^{-1}$)[b]	I_{DS-1}/I_{DS-0}[c]	ΔV_T (V) (V_P/V_E)	retention time (s)
Si/SiO_2	PS/PVA/PMMA	40/120/320	0.18	10^4	25.3 (±70 V)	10^8
	PVA/PMMA	140/320	3.4×10^{-3}	15	48.5 (±60 V)	<50
	PS/PMMA	40/320	0.31		negligible	
	PMMA/PVA/PMMA	35/125/320	0.10	250	24.6 (±70 V)	10^7
	PS/PVA/P(VDF-TrFE-CFE)	20/120/180	0.25	3×10^4	19.1 (±30 V)	7×10^3
		30/120/180	0.24	10^4	15.2 (±30 V)	4×10^5
		40/120/180	0.26	2×10^4	9.7 (±30 V)	10^8
		55/120/180	0.19	2×10^4	9.1 (±30 V)	10^9
PES	PS/PVA/PMMA	55/120/200	3.8×10^{-2}	2×10^4	15.4 (±50 V)	10^8
	PS/PVA/P(VDF-TrFE-CFE)	40/120/380	1.1×10^{-2}	3×10^3	10.0 (±30 V)	10^8

[a]Channel W/L = 1000 μm/100 μm. [b]Only electron mobility was shown, calculated from the linear region at V_{DS} = 5 V. [c]On/off memory current ratios were extracted at $V_R = V_{GS}$ = 0 V and V_{DS} = 5 V.

where Q and C_i are the stored charge density in the PVA layer and the capacitance per unit area of the gate dielectrics, respectively. As a result, the stored charge density was estimated to be approximately 1.2×10^{12} cm^{-2} with a ΔV_T of 25.3 V at the V_{GS} sweeping range of ±70 V. Both negative and positive V_T obtained at the forward and reverse V_{GS} sweeping direction, respectively, are in principle advantageous for high on/off memory current ratio at a reading voltage (V_R) of V_{GS} = 0 V. As a result, an on/off memory current ratio (I_{DS-1}/I_{DS-0}, the ratio of the I_{DS} at the "1" state and the I_{DS} at "0" state) larger than 10^4 was achieved at V_R = 0 V and a V_{GS} sweeping range of ±70 V.

The reliability of our device was examined with time-dependent data retention performance. After supplying a programming voltage (V_P) and erasing voltage (V_E) of V_{GS} = ±70 V for 1 s, respectively, the reading current at both "1" and "0" states was recorded as the function of the time at a time interval of 200 s at $V_R = V_{GS}$ = 0 V and V_{DS} = 5 V. During the periods of V_P/V_E operations, the V_{DS} was kept at 0 V. Both "1" and "0" states maintained well, with the I_{DS-1}/I_{DS-0} always being larger than 10^3 during the measurement range of 4400 s, as shown in Figure 1c. After the initial degradation, the I_{DS} at both "1" and "0" states could be approximately fitted as a linear relationship with the time in the double logarithm coordinate system as shown by the black and red lines, respectively, in Figure 1c. On the basis of the fitted results, the I_{DS-1}/I_{DS-0} was maintained as higher than 1 order of magnitude after 10^8 s (Figure 1c), which is higher than the values reported by previous OTFT-NVM devices.[6,13,14,19,24] The excellent data retention is mainly attributed to the 40-nm-thick, smooth, and free-pinhole PS tunneling layer, which efficiently reduced the leakage of the trapped charges from the PVA layer to the channel.

A control device without a PS layer exhibited a poor device performance, with low on/off current ratio and short memory retention (Figure S2a,d, SI). In particular, due to the many hydroxyl groups of the PVA layer in direct contact with P(NDI2OD-T2) serving as electron trap sites, the OTFT with the PVA/PMMA bilayer dielectric exhibits a very poor electron mobility of approximately 3.4×10^{-3} $cm^2\ V^{-1}\ s^{-1}$, resulting in a very small I_{DS-1}/I_{DS-0} of 15 at V_{GS} = 0 V (Figure S2a, SI). When a 35-nm-thick PMMA dielectric was used as the tunneling layer instead of PS, a similar memory and data retention but a relatively small I_{DS-1}/I_{DS-0} of about 250 (at V_R = 0 V) at V_{GS} sweeping range of ±70 V were observed, which again consolidates the importance of a tunneling layer (Figure S3b, SI). The small current ratio may be due to the low field effect electron mobility of the device at the PMMA/P(NDI2OD-T2) interface. As summarized in Table 1, all memory devices prepared on the Si substrate with PS as the tunneling layer showed a reasonably high μ_e of about 0.2 $cm^2\ V^{-1}\ s^{-1}$, while the memory device with the PMMA tunneling layer showed a relatively low μ_e of 0.10 $cm^2\ V^{-1}\ s^{-1}$.

The voltage of V_P/V_E = ±70 V required to operate the device was much higher than that of FG-NVMs based on inorganic semiconductor. The high operation voltage is also one of the most common problems in OTFTs, and mainly two strategies have been used to reduce the operation voltage: using a thinner low-κ dielectric layer[33,34] or a thicker high-κ dielectric layer.[35,36] For successful low-voltage operation of our OTFT-NVM, the voltage applied should be minimized to build sufficient electric field (E_T) in the PS tunneling layer to ensure the efficient injection of ambipolar charge from semiconductor into PVA. At the initial stage of memory operation (no charges stored in the PVA layer), the built electric field (E_T) in the tunneling layer can be estimated from the equation

$$E_T = V_{GS}/[d_1 + d_2(\kappa_1/\kappa_2) + d_3(\kappa_1/\kappa_3)] \quad (4)$$

where d_1, d_2, d_3 and κ_1, κ_2, κ_3 are the thicknesses and the dielectric constants of tunneling, charge-trapping, and blocking layers, respectively. The smaller d_3 or the higher κ_3 favors the induction of E_T at a relatively low V_P/V_E. When either a thin low-κ (~3.5) PMMA (200 nm) dielectric or a relatively thick high-κ (~60)[36] P(VDF-TrFE-CFE) (380 nm) dielectric was employed as a blocking layer with a 40-nm-thick PS tunneling layer, a large memory window of ΔV_T = 19.8 or 18.7 V was obtained, respectively, at the significantly low V_P/V_E of ±40 V (Figure S4, SI).

Great care should be taken to further reduce the operation voltage by decreasing blocking layer thickness. A device with a blocking P(VDF-TrFE-CFE) layer thinner than 100 nm shows poor transfer characteristics. The $I_{DS}-V_{GS}$ curve showed relatively small hysteresis with two different directions, i.e., an anticlockwise direction at lower negative and positive V_{GS} and a clockwise direction at higher negative and positive V_{GS}, due to the charge injection from the gate into the PVA layer through the tunneling to the thin blocking layer, giving rise to substantial leakage current (I_{GS}) (Figure S5, SI). By considering these counteracting factors, the blocking layer should be optimized to minimize the operation voltage. The blocking layer plays an important role in the OTFT-NVM by preventing charge transfer from the gate to the PVA layer or vice versa, so

DOI: 10.1021/acsami.5b02213
ACS Appl. Mater. Interfaces 2015, 7, 10957−10965

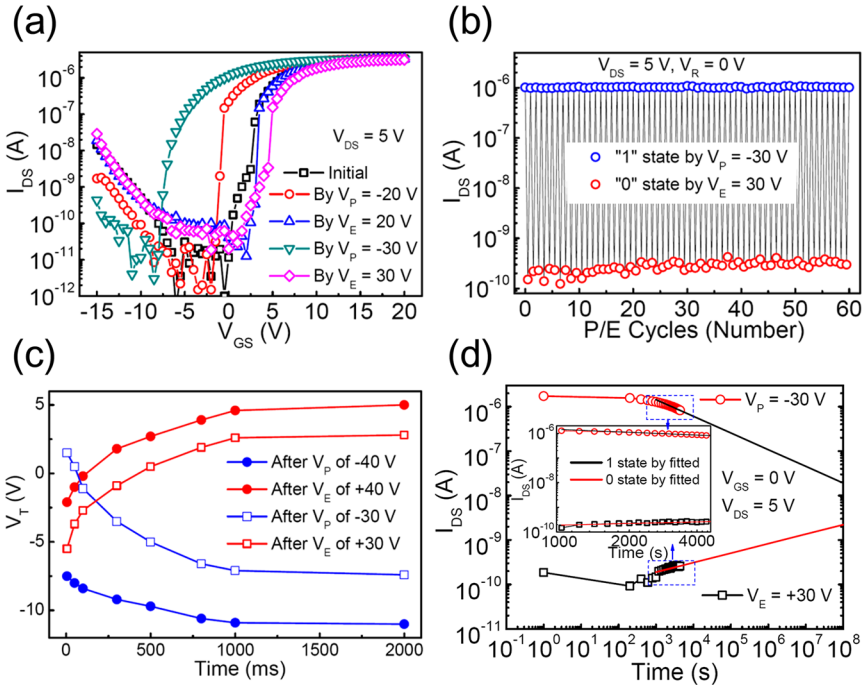


Figure 2. Memory characteristics of an OTFT-NVM with PS (40 nm)/PVA/PVDF-TrFE-CFE (180 nm) multilayers on a Si substrate. (a) Transfer characteristics of memory before/after the corresponding programming and erasing operations, respectively. (b) Cycling endurance characterisitcs of the memory. (c) Programming and erasing speeds of the device by the supplied V_P/V_E of ±30 and ±40 V, respectively. (d) Memory retention characteristics at both "1" and "0" states. The inset of d shows a magnified display of the experimental data up to 4600 s and fitted data of retention characteristics.

it should have a proper thickness to get a reasonably low operation voltage and prominent memory effect with good retention ability.

An OTFT-NVM with 40-nm-thick PS tunneling and 180-nm-thick P(VDF-TrFE-CFE) blocking layers exhibits excellent memory characteristics at the low V_P/V_E of ±20 V, as shown in Figure 2a. An initial transfer curve of the memory was first recorded with V_{GS} sweeping from −15 to 20 V at V_{DS} of 5 V, prior to the supply of any V_P/V_E. The elementary performance parameters of the device operated in n-channel mode, such as μ_e, on/off current ratio, V_T, and SS, were calculated to be approximately 0.26 $cm^2 V^{-1} s^{-1}$, 3×10^5, 0.6, and 0.7 V/decade, respectively, in the linear region, from the initial transfer curve.

After V_P/V_E were supplied for 1 s, the transfer curves were recorded again at the same condition as that of the initial transfer curve. The transfer curve had an obvious negative shift (V_T = −1.3 V) after the V_P of −20 V. The negatively shifted transfer curve was returned to the initial state (V_T = 0.7 V) after an opposite polarity V_E of 20 V was supplied for 1 s. Moreover, the transfer curve was more shifted in both negative (V_T = −7.1 V) and positive (V_T = 2.6 V) directions after the corresponding increased V_P (=−30 V) and V_E (=30 V), respectively. The similar slopes of all transfer curves in Figure 2a suggested that μ_e of the device was independent of V_P/V_E. The ΔV_T of 9.7 V, the stored charge density of approximately 1.6×10^{12} cm^{-2} in the PVA layer, and the $I_{DS\text{-}1}/I_{DS\text{-}0}$ of approximately 2×10^4 (at V_R = 0 V) were achieved by V_P/V_E = ±30 V. For P(NDI2OD-T2) with hole and electron as minority and majority carrier, respectively, the reversible bidirectional shifts of the programmed/erased V_T from the initial state indicates that both holes and electrons were injected and trapped in the PVA layer by the corresponding V_P/V_E, respectively. Considering the LUMO (−4.0 eV) and HOMO (−5.6 eV) of P(NDI2OD-T2) and the LUMO (−0.4 eV) and HOMO (−6.95 eV) of PS, the barrier of electrons between P(NDI2OD-T2) and PS is 3.6 eV, which is greater than that of hole (1.35 eV). The injection of electron from P(NDI2OD-T2) into PVA by tunneling PS is, therefore, more difficult than that of holes, which implies that hole trapping is more significant than electron trapping in our memory. More prominent shifts of the programmed V_T than that of the erased V_T at symmetric V_P/V_E confirms our argument.

The memory cycling endurance characteristics of the memory were measured by applying continuous dynamic cyclic voltages of $V_P/V_R/V_E/V_R$ = −30/0/+30/0 V, with the V_{DS} defined as 0 and 5 V during the program/erase (P/E) and reading (R) periods, respectively, as shown in Figure 2b. The results show reversible and reliable memory-cycle behavior over more than 60 cycles with distinguished I_{DS} between "1" and "0" states greater than 10^3. As shown in Figure 2c, the effect of the pulse time of different V_P/V_E on the V_T of the memory device was measured. Before each programmed (erased) V_T was measured, the memory device was reset to the erased (programmed) state by supplying V_E (V_P) for a long enough time of 2 s. The V_T of the device was gradually shifted in the negative (positive) direction from the erased (programmed) state by increasing the pulse time with V_P of −30 and −40 (V_E of +30 and +40) V for programming (erasing) operations, respectively. For V_P/V_E of ±30 V, at least 300 ms switch time was typically needed to fully program or erase the memory device. On the other hand, 5 ms (the shortest pulse time supplied by our measurement equipment) was sufficient to fully program or erase the memory device by V_P/V_E of ±40 V.

The retention ability of the memory was examined with the I_{DS} in both "1" and "0" states as the function of time with a time interval of 200 s, at the reading state of V_{GS} = 0 V and V_{DS} = 5

DOI: 10.1021/acsami.5b02213
ACS Appl. Mater. Interfaces 2015, 7, 10957−10965

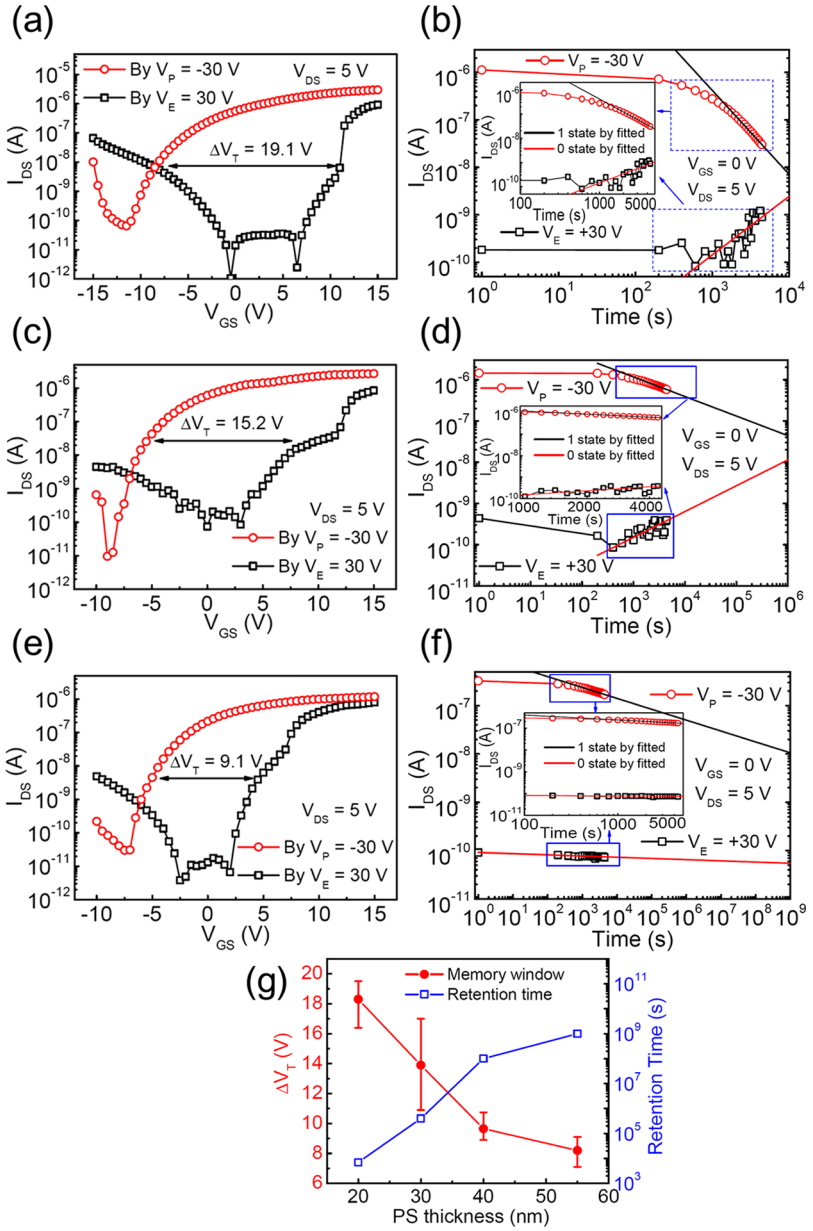


Figure 3. Transfer characteristics of the memory devices with (a) 20-nm-thick, (c) 30-nm-thick, and (e) 55 nm-thick PS tunneling layers. Retention characteristics of the memory devices with (b) 20-nm-thick, (d) 30-nm-thick, and (f) 55-nm-thick PS tunneling layers. The insets of parts b, d, and f show a magnified display of part of the experimental data and fitted data of retention characteristics. P(VDF-TrFE-CFE) blocking layers that were 180 nm thick were used in all the devices on Si substrates. (g) Memory window and the retention time as a function of the PS tunneling-layer thickness.

V, after the corresponding V_P/V_E = ±30 V were supplied for 1 s, respectively, as shown in Figure 2d. In the measurement range, both states were maintained well, with the $I_{DS\text{-}1}/I_{DS\text{-}0}$ being larger than 3 × 10^3. The extrapolation of the results implies that the memory ratio could be maintained at 1 order of magnitude after 10^8 s, as shown in Figure 2d. It is common to observe the decrease and increase of on-state I_{DS} and the off-state I_{DS} during the retention measurement, respectively, due to the degradation of the trapped charges with time. In our system, the loss of the trapped holes (or electrons) with the time makes the number of accumulated (or depleted) electrons in the n-type channel decreased, giving rise to the decrease of on state I_{DS} (or the increase of off-state I_{DS}) with time. As described previously, the injection of electron is more difficult than that of holes, making hole trapping more significant than electron trapping in our memory. Since the amount of holes trapped in PVA was larger than that of electrons by the symmetric V_P/V_E, the built-up potential after programmed operations (hole trapping) may be greater than that after erased operations (electron trapping). The higher potential upon hole trapping resulted in the faster decrease of the on state I_{DS} during the measurement of retention, as shown in Figure 2d.

Another way to control the memory performance of our device, such as V_P/V_E and ΔV_T, is to vary the thickness of the PS tunneling layer, as expected from the relation of E_T with d_1 in eq 2. The effect of the thickness of the PS tunneling layer on the performances of memory devices is shown in Figure 3. When a very thin PS layer of approximately 20 nm was used, a large ΔV_T of 19.1 V was achieved at V_P/V_E of ±30 V, as shown in Figure 3a. The enlarged ΔV_T results from the larger E_T built

DOI: 10.1021/acsami.5b02213
ACS Appl. Mater. Interfaces 2015, 7, 10957−10965

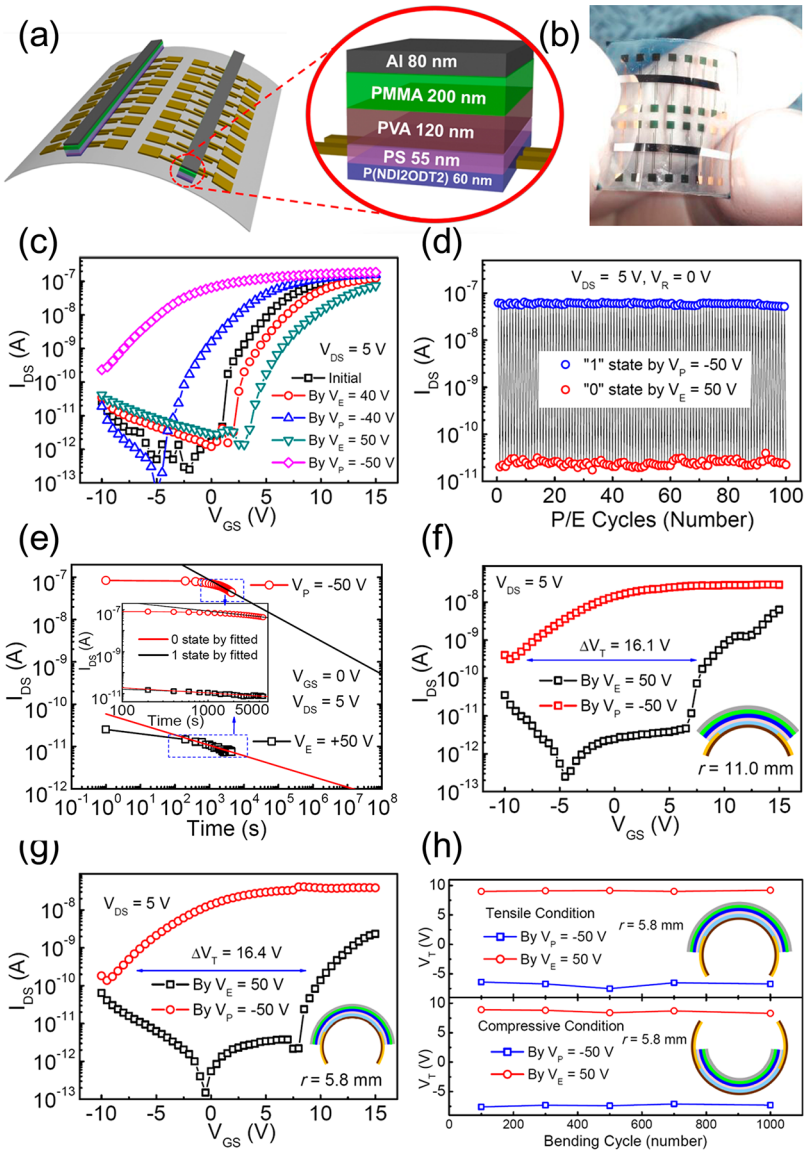


Figure 4. (a) Schematic configuration and (b) photograph of arrays of flexible OTFT-NVMs on a PES substrate. (c) Transfer characteristics of a memory before/after the corresponding V_P/V_E operations, respectively. (d) Cycling endurance characterisitcs of the memory. (e) Retention characteristics at both "1" and "0" states of the flexible memory at the flat state. Transfer characteristics of the flexible memory after V_P/V_E operations for the tensile bending conditions of (f) r = 11.0 mm and (g) r = 5.8 mm, respectively. (h) The programmed and erased V_T of the flexible memory at the flat condition after selected tensile and compressive bending cycles. The inset of part e shows a magnified display of the experimental data up to 5000 s and fitted data of retention characteristics. The insets of parts f, g, and h show schematic illustrations of the memory device under tensile or compressive conditions, respectively.

in the PS layer at the same V_P/V_E, which again allows for more electrons and holes to be injected into and trapped in the PVA layer. However, the memory retention was substantially deteriorated and the device fails to work after approximately 7000 s, as shown in Figure 3b. When a 30-nm-thick PS tunneling layer was employed, the ΔV_T of the device decreased to 15.2 V at V_P/V_E of ±30 V (Figure 3c), but the retention time was prolonged to approximately 4×10^5 s (Figure 3d). The results clearly suggest that there is a trade-off between ΔV_T and data retention that depends on the PS thickness. After optimization of the PS layer thickness, we were able to develop an OTFT-NVM with a 55-nm-thick PS layer that exhibited a reasonably large ΔV_T of 9.1 V (V_P/V_E of ±30 V) with extremely long data retention over 10^9 s, as shown in parts e and f of Figure 3, respectively. The detailed memory properties of the memory devices are summarized in Table 1, and the trade-off relation between ΔV_T and data retention as a function of the PS thickness is shown in Figure 3g. We also examined the effect of PVA thickness on the memory performance. A memory device with a thickness of PVA of approximately 80 nm prepared from a solution with a concentration of 3.0 wt % exhibited a memory window smaller than that of the devices with a 120-nm-thick PVA layer (Figure S6, SI). A uniform PVA film was hardly obtained when a PVA solution was used with a concentration below 2.0 wt % under our experimental conditions.

A benefit of our OTFT-NVM with all-polymer semiconducting, tunneling, charge-trapping and blocking layers is its mechanical flexibility. A flexible OTFT-NVM memory was developed on a transparent 120-μm-thick poly(ether sulfone) (PES) substrate, as schematically shown in Figure 4a. The arrays of devices in Figure 4b again exhibit transfer character-

DOI: 10.1021/acsami.5b02213
ACS Appl. Mater. Interfaces 2015, 7, 10957−10965

istics similar to those observed in a device on Si substrate before and after V_P/V_E, as shown in Figure 4c. The detailed elementary performance at n-channel mode, calculated from the initial transfer curve, is however a little worse than that on Si substrate, possibly due to the rough PES surface (as shown in Figure S1, SI). A μ_e of 3.8×10^{-2} cm^2 V^{-1} s^{-1}, an on/off current ratio of about 3×10^5, a V_T of 2.6 V, and a SS of 2.0 V/decade in the linear region were obtained. The prominent memory characteristics were also achieved, with a memory window of 15.4 V and a high $I_{DS\text{-}1}/I_{DS\text{-}0}$ of 2×10^4 (V_R = 0 V) at a V_P/V_E of ±50 V.

The memory cycling endurance for the flexible memory was investigated with a series of repeated dynamic cyclic of $V_P/V_R/V_E/V_R$ = −50/0/+50/0 V, with the V_{DS} defined as 0 and 5 V during the P/E and R periods, respectively, and the results are shown in Figure 4d. Reversible and stable memory-cycle behavior was obtained for more than 100 cycles with distinguished I_{DS} between "1" and "0" states for about 3×10^3. After supplying V_P/V_E = ±50 V, the measured retention characteristics of the flexible memory also showed that the memory current ratio of 5×10^3 was well-maintained after 4400 s. The fitted results indicate good retention ability, with a memory ratio larger than 1 order of magnitude, even after 10^8 s in the flexible memory, as shown in Figure 4e.

Moreover, the device stability under mechanical deformation is an important property to make our OTFT-NVM potentially suitable for flexible electronics. The transfer characteristics of a memory on a PES substrate after supplying V_P/V_E = ±50 V were measured in the cases of tensile bending states with a radius (r) of 11.0 and 5.8 mm, respectively, as shown in parts f and g of Figure 4. The memory windows were negligibly changed, irrespective of bending radius. However, the device bent with r = 5.8 mm exhibits a lower on current than that for the flat state, giving rise to the reduced $I_{DS\text{-}1}/I_{DS\text{-}0}$ of approximately 10^4. The bending endurance test was carried out by repetitively bending a device at r = 5.8 mm. Both programmed and erased V_T values were recorded in the flat state after the selected cycles. As a result, the flexible memory device exhibited almost no change in V_T at both states even after 1000 bending cycles, as shown in Figure 4h.

Autoencapsulation of the air-sensitive semiconducting layer with the overlaid gate insulators and gate electrode in top-gate configuration beneficially makes the present flexible OTFT-NVM device environmentally stable. The device had worked well after storage in the lab (in ambient atmosphere, at room temperature and a relatively humidity of 20%) for 20 days, with a memory window of 13.5 V, $I_{DS\text{-}1}/I_{DS\text{-}0}$ near 10^4 (V_R = 0 V), and retention time of about 10^8 s with V_P/V_E = ±50 V (Figure S7, SI). Furthermore, a flexible OTFT-NVM with low operation voltage was successfully fabricated with high-κ P(VDF-TrFE-CFE) blocking layer on a PES substrate. The prominent memory properties were achieved with a memory window of 10.0 V, $I_{DS\text{-}1}/I_{DS\text{-}0}$ of about 3×10^3 ($V_R = V_{GS}$ = 0 V), and retention time of the $I_{DS\text{-}1}/I_{DS\text{-}0}$ larger than 1 order of magnitude after 10^8 s with V_P/V_E = ±30 V (Figure S8, SI).

4. CONCLUSION

We developed a novel, nonvolatile, thin-film transistor memory with a solution-processed polymer electret as charge-trapping layer in which holes and electrons of a semiconducting P(NDI2OD-T2) polymer were reversibly programmed and erased, dependent upon gate voltage. To ensure reliable charge injection, storage, and removal during memory operation, additional tunneling and blocking polymer layers were employed on the bottom and top of the charge-trapping layer, respectively. Device performance was systematically examined as a function of the thickness of both the tunneling and blocking layers, and under optimized conditions, a OTFT-NVM exhibited a high on/off memory ratio >10^4 and a long retention time of 10^8 s. Our device with four polymer semiconducting, tunneling, charge-trapping, and blocking layers prepared by sequential spin-coating of each polymer was also fabricated on a flexible polymer substrate, giving rise to excellent memory performance with high memory margin, long retention, and write/read cycle endurance, even after multiple bending events.

■ ASSOCIATED CONTENT

Supporting Information

AFM images and $I-V$ characteristics results. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.5b02213.

■ AUTHOR INFORMATION

Corresponding Author

*Tel 82-2-2123-2833. Fax: 82-2-312-5375. E-mail: cmpark@yonsei.ac.kr.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This research was supported by the third Stage of the Brain Korea 21 Plus Project in 2014 and National Research Foundation of Korea (NRF) grant funded by the Korean government (MEST) (No. 2014R1A2A1A01005046) and the Pioneer Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning (2010-0019313).

■ REFERENCES

(1) Baegm, K.-J.; Noh, Y.-Y.; Sirringhaus, H.; Kim, D.-Y. Controllable Shifts in Threshold Voltage of Top-Gate Polymer Field-Effect Transistors for Applications in Organic Nano Floating Gate Memory. *Adv. Funct. Mater.* **2010**, *20*, 224−230.

(2) Wang, W.; Ma, D. Organic Floating-Gate Transistor Memory Based on The Structure of Pentacene/Nanoparticle-Al/Al_2O_3. *Appl. Phys. Lett.* **2010**, *96*, 203304.

(3) Wang, S. M.; Leung, C. W.; Chan, P. K. L. Nonvolatile Organic Transistor-Memory Devices Using Various Thicknesses of Silver Nanoparticle Layers. *Appl. Phys. Lett.* **2010**, *97*, 023511.

(4) Kaltenbrunner, M.; Stadler, P.; Schwödiauer, R.; Hassel, A. W.; Sariciftci, N. S.; Bauer, S. Anodized Aluminum Oxide Thin Films for Room-Temperature-Processed, Flexible, Low-Voltage Organic Non-Volatile Memory Elements with Excellent Charge Retention. *Adv. Mater.* **2011**, *23*, 4892−4896.

(5) Li, J.; Yan, F. Solution-Processable Low-Voltage and Flexible Floating-gate Memories Based on an n-Type Polymer Semiconductor and High-κ Polymer Gate Dielectrics. *ACS Appl. Mater. Interfaces* **2014**, *6*, 12815−12820.

(6) Kim, S.-J.; Park, Y.-S.; Lyu, S.-H.; Lee, J.-S. Nonvolatile Nano-Floating Gate Memory Devices Based on Pentacene Semiconductors and Organic Tunneling Insulator Layers. *Appl. Phys. Lett.* **2010**, *96*, 033302.

(7) Han, S.-T.; Zhou, Y.; Wang, C.; He, L.; Zhang, W.; Roy, V. A. L. Layer-by-Layer-Assembled Reduced Graphene Oxide/Gold Nanoparticle Hybrid Double-Floating-Gate Structure for Low-Voltage Flexible Flash Memory. *Adv. Mater.* **2013**, *25*, 872−877.

DOI: 10.1021/acsami.5b02213
ACS Appl. Mater. Interfaces 2015, 7, 10957−10965

(8) Zhou, Y.; Han, S.-T.; Sonar, P.; Roy, V. A. Nonvolatile Multilevel Data Storage Memory Device from Controlled Ambipolar Charge Trapping Mechanism. *Sci. Rep.* **2013**, *3*, 2319.
(9) Chen, C.-M.; Liu, C.-M.; Wei, K.-H.; Jeng, U.-S.; Sub, C.-H. Non-Volatile Organic Field-Effect Transistor Memory Comprising Sequestered Metal Nanoparticles in a Diblock Copolymer Film. *J. Mater. Chem.* **2012**, *22*, 454−461.
(10) Wei, Q.; Lin, Y.; Anderson, E. R.; Briseno, A. L.; Gido, S. P.; Watkins, J. J. Additive-Driven Assembly of Block Copolymer−Nanoparticle Hybrid Materials for Solution Processable Floating Gate Memory. *ACS Nano* **2012**, *6*, 1188−1194.
(11) Han, S.-T.; Zhou, Y.; Xu, Z.-X.; Huang, L.-B.; Yang, X.-B.; Roy, V. A. L. Microcontact Printing of Ultrahigh Density Gold Nanoparticle Monolayer for Flexible Flash Memories. *Adv. Mater.* **2012**, *24*, 3556−3561.
(12) Han, S.-T.; Zhou, Y.; Xu, Z.-X.; Roy, V. A. L. T.; Hung, F. Nanoparticle Size Dependent Threshold Voltage Shifts in Organic Memory Transistors. *J. Mater. Chem.* **2011**, *21*, 14575−14580.
(13) Kim, S.-J.; Lee, J.-S. Flexible Organic Transistor Memory Devices. *Nano Lett.* **2010**, *10*, 2840−2890.
(14) Baeg, K.-J.; Khim, D.; Kim, J.; Yang, B.-D.; Kang, M.; Jung, S.-W.; You, I.-K.; Kim, D.-Y.; Noh, Y.-Y. High-Performance Top-Gated Organic Field-Effect Transistor Memory Using Electrets for Monolithic Printed Flexible NAND Flash Memory. *Adv. Funct. Mater.* **2012**, *22*, 2915−2926.
(15) Baeg, K.-J.; Noh, Y.-Y.; Ghim, J.; Kang, S.-J.; Lee, H.; Kim, D.-Y. Organic Non-Volatile Memory Based on Pentacene Field-Effect Transistors using a Polymeric Gate Electret. *Adv. Mater.* **2006**, *18*, 3179−3183.
(16) Yeh, B.-L.; Chen, Y.-H.; Chiu, L.-Y.; Lin, J.-W.; Chen, W.-Y.; Chen, J.-S.; Chou, T.-H.; Chou, W.-Y.; Tang, F.-C.; Cheng, H.-L. Organic Nonvolatile Memory Based on Low Voltage Organic Thin Film Transistors with Polymer Gate Electrets. *J. Electrochem. Soc.* **2011**, *158*, H277−H280.
(17) Dao, T. T.; Matsushima, T.; Murata, H. Organic Nonvolatile Memory Transistors Based on Fullerene and an Electron-Trapping Polymer. *Org. Electron.* **2012**, *13*, 2709−2715.
(18) Chen, C.-M.; Liu, C.-M.; Tsai, M.-C.; Chen, H.-C.; Wei, K.-H. A Nanostructured Micellar Diblock Copolymer Layer Affects the Memory Characteristics and Packing of Pentacene Molecules in Non-Volatile Organic Field-Effect Transistor Memory Devices. *J. Mater. Chem. C* **2013**, *1*, 2328−2337.
(19) Kim, B. J.; Ko, Y.; Cho, J. H.; Cho, J. Organic Field-Effect Transistor Memory Devices Using Discrete Ferritin Nanoparticle-Based Gate Dielectrics. *Small* **2013**, *9*, 3784−3791.
(20) Tsai, T.-D.; Chang, J.-W.; Wen, T.-C.; Guo, T.-F. Manipulating the Hysteresis in Poly(vinyl alcohol)−Dielectric Organic Field-Effect Transistors toward Memory Elements. *Adv. Funct. Mater.* **2013**, *23*, 4206−4214.
(21) Wang, W.; Han, J.; Ying, J.; Xiang, L.; Xie, W. Effect of Tunneling Layers on the Performances of Floating-Gate Based Organic Thin-Film Transistor Nonvolatile Memories. *Appl. Phys. Lett.* **2014**, *105*, 123303.
(22) Chiu, Y.-C.; Chen, T.-Y.; Chen, Y.; Satoh, T.; Kakuchi, T.; Chen, W.-C. High-Performance Nonvolatile Organic Transistor Memory Devices Using the Electrets of Semiconducting Blends. *ACS Appl. Mater. Interfaces* **2014**, *6*, 12780−12788.
(23) Chou, Y.-H.; Chang, H.-C.; Liu, C.-L; Chen, W.-C. Polymeric Charge Storage Electrets for Non-Volatile Organic Field Effect Transistor Memory Devices. *Polym. Chem.* **2015**, *6*, 341−352.
(24) Kang, M.; Baeg, K.-J.; Khim, D.; Noh, Y.-Y.; Kim, D.-Y Printed, Flexible, Organic Nano-Floating-Gate Memory: Effects of Metal Nanoparticles and Blocking Dielectrics on Memory Characteristics. *Adv. Funct. Mater.* **2013**, *23*, 3503−3512.
(25) Leong, W. L.; Mathews, N.; Tan, B.; Vaidyanathan, S.; Dötz, F.; Mhaisalkar, S. Solution Processed Non-Volatile Top-Gate Polymer Field-Effect Transistors. *J. Mater. Chem.* **2011**, *21*, 8971−8974.
(26) Yan, H.; Chen, Z. H.; Zheng, Y.; Newman, C.; Quinn, J. R.; Dötz, F.; Kastler, M. A High-Mobility Electron-Transporting Polymer for Printed Transistors. *Nature* **2009**, *457*, 679−687.
(27) Baeg, K.-J.; Khim, D.; Jung, S.-W.; Kang, M.; You, I.-K.; Kim, D.-Y.; Facchetti, A.; Noh, Y. Y. Remarkable Enhancement of Fole Transport in Top-Gated n-Type Polymer Field-Effect Transistors by a High-κ Dielectric for Ambipolar Electronic Circuits. *Adv. Mater.* **2012**, *24*, 5433−5439.
(28) Debucquoy, M.; Rockelé, M.; Genoe, J.; Gelinck, G. H.; Heremans, P. Charge Trapping in Organic Transistor Memories: On the Role of Electrons and Holes. *Org. Electron.* **2009**, *10*, 1252−1258.
(29) Bhargav, P. B.; Mohan, V. M.; Sharma, A. K.; Rao, V. V. R. N. Investigations on Electrical Properties of (PVA:NaF) Polymer Electrolytes for Electrochemical Cell Applications. *Curr. Appl. Phys.* **2009**, *9*, 165−171.
(30) Salavagione, H. J.; Martínez, G.; Gómez, M. A. Synthesis of Poly(vinyl alcohol)/Reduced Graphite Oxide Nanocomposites with Improved Thermal and Electrical Properties. *J. Mater. Chem.* **2009**, *19*, 5027−5032.
(31) Baeg, K.-J.; Noh, Y.-Y.; Ghim, J.; Lim, B.; Kim, D.-Y. Polarity Effects of Polymer Gate Electrets on Non-Volatile Organic Field-Effect Transistor Memory. *Adv. Funct. Mater.* **2008**, *18*, 3678−3685.
(32) Wang, W.; Ma, D.; Pan, S.; Yang, Y. Hysteresis Mechanism in Low-Voltage and High Mobility Pentacene Thin-Film Transistors with Polyvinyl Alcohol Dielectric. *Appl. Phys. Lett.* **2012**, *101*, 033303.
(33) Halik, M.; Klauk, H.; Zschieschang, U.; Schmid, G.; Dehm, C.; Schütz, M.; Maisch, S.; Effenberger, F.; Brunnbauer, M.; Stellacci, F. Low-Voltage Organic Transistors with an Amorphous Molecular Gate Dielectric. *Nature* **2004**, *431*, 963−966.
(34) Walser, M. P.; Kalb, W. L.; Mathis, T.; Batlogg, B. Low-Voltage Organic Transistors and Inverters with Ultrathin Fluoropolymergate Dielectric. *Appl. Phys. Lett.* **2009**, *95*, 233301.
(35) Dimitrakopoulos, C. D.; Purushothaman, S.; Kymissis, J.; Callegari, A.; Shaw, J. M. Low-Voltage Organic Transistors on Plastic Comprising High-Dielectric Constant Gate Insulators. *Science* **1999**, *283*, 822−824.
(36) Li, J.; Sun, Z.; Yan, F. Low-Voltage Organic Thin Film Transistors with High-*k* Relaxor Ferroelectric Polymer as Gate Insulator. *Adv. Mater.* **2012**, *24*, 88−93.

DOI: 10.1021/acsami.5b02213
ACS Appl. Mater. Interfaces 2015, 7, 10957−10965